programmable logic device, [and changes] to change the encrypting circuit with an existing mapping data object [as the change data].

3. (ONCE AMENDED) The encrypting apparatus as set forth in claim 1,

wherein said changing [means] unit includes:

a compiler [means for generating] unit to generate a mapping data object [that represents] representing the structure of the encrypting circuit, by compiling a library written in a hardware description language, and

a configuration [means for writing] unit to write the mapping data object to the programmable logic device; and

wherein said changing [means] unit reads an existing library [as] to obtain the change data, compiles the existing library, and changes the encrypting circuit.

4. (ONCE AMENDED) The encrypting apparatus as set forth in claim 1,

wherein said changing [means] unit includes:

a database [means for storing] unit to store an encrypting algorithm file having a predetermined encrypting algorithm,

a compiler [means for generating] unit to generate a mapping data object [that represents] representing the structure of the encrypting circuit, by compiling a library written in a hardware description language, and

a configuration [means] unit for writing the mapping data object to the programmable logic device; and

wherein said changing [means] unit receives the change data from outside said encrypting apparatus, retrieves a relevant encrypting algorithm file and changes the encrypting circuit with the library in the relevant encrypting algorithm file, corresponding to setup data given as the change data [from the outside].

5. (ONCE AMENDED) The encrypting apparatus as set forth in claim 1,

further comprising[:] a network connecting [means for connecting] unit to connect the encrypting apparatus to a communication network, and

wherein said changing [means] unit reads the change data from the communication network.

6. (ONCE AMENDED) The encrypting apparatus as set forth in claim 5, wherein said network connecting [means] unit receives [the] encrypted change data from the

communication network, and said changing [means] unit changes the encrypting circuit corresponding to the encrypted change data.

7. (ONCE AMENDED) The encrypting apparatus as set forth in claim 1, wherein said changing [means] unit periodically updates the encrypting specifications.

8. (ONCE AMENDED) The encrypting apparatus as set forth in claim 1, wherein said changing [means] unit updates the encrypting specifications corresponding to an external command.

9. (ONCE AMENDED) The encrypting apparatus as set forth in claim 1, wherein said changing [means] unit changes the encrypting specifications corresponding to at least one of a communication path of data to be encrypted, a degree of security thereof, and a process speed required therefor.

10. (TWICE AMENDED) A decrypting apparatus, comprising:

a circuit [means] unit, having at least one programmable logic device, [for forming] to form a decrypting circuit with the programmable logic device corresponding to given decrypting specifications; and

a changing [means for reading] unit, coupled to said circuit unit, to read change data for changing the decrypting specifications and to change automatically [changing] a structure of the decrypting circuit corresponding to the change data by changing a circuit structure of the programmable logic device without removal from said decrypting apparatus.

11. (ONCE AMENDED) The decrypting apparatus as set forth in claim 10, wherein said changing [means] unit includes a configuration [means for writing] unit to write a mapping data object [that represents] representing the structure of the decrypting circuit to the programmable logic device, [and changes] to change the decrypting circuit with an existing mapping data object [as the change data].

12. (ONCE AMENDED) The decrypting apparatus as set forth in claim 10, wherein said changing [means] unit includes:

a compiler [means for generating] unit to generate a mapping data object [that represents] representing the structure of the decrypting circuit, by compiling a library written in a hardware description language, and

a configuration [means for writing] unit to write the mapping data object to the programmable logic device; and

wherein said changing [means] unit reads an existing library [as] to obtain the change data, compiles the existing library, and changes the decrypting circuit.

13. (ONCE AMENDED) The decrypting apparatus as set forth in claim 10,

wherein said changing [means] unit includes:

a database [means for storing] unit to store a decrypting algorithm file having a predetermined decrypting algorithm,

a compiler [means for generating] unit to generate a mapping data object [that represents] representing the circuit structure of the decrypting circuit, by compiling a library written in a hardware description language, and

a configuration [means] unit for writing the mapping data object to the programmable logic device; and

wherein said changing [means] unit receives the change data from outside said decrypting apparatus, retrieves a relevant decrypting algorithm file and changes the decrypting circuit with the library in the relevant decrypting algorithm file, corresponding to setup data given as the change data [from the outside].

14. (ONCE AMENDED) The decrypting apparatus as set forth in claim 10,

further comprising[:] a network connecting [means for connecting] unit to connect the decrypting apparatus to a communication network, and

wherein said changing [means] unit reads the change data from the communication network.

15. (ONCE AMENDED) The decrypting apparatus as set forth in claim 14,

wherein said network connecting [means] unit receives [the] decrypted change data from the communication network, and

wherein said changing [means] unit changes the decrypting circuit corresponding to the decrypted change data.

16. (ONCE AMENDED) The decrypting apparatus as set forth in claim 10, wherein said changing [means] unit periodically updates the decrypting specifications.